AMENDMENTS TO THE CLAIMS

1-26. (Canceled).

27. (Currently amended) An array of resistance variable memory cells comprising:

at least one pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode, a chalcogenide glass layer having metal ions diffused therein in contact with the first electrode and being capable of changing resistance under the influence of an applied voltage, a metal layer in contact with the chalcogenide glass layer, and a second electrode in contact with the metal layer, wherein the second electrode and metal layer comprise different materials~~, the at least one pillar not located within a via~~.

28-48. (Canceled).

49. (Previously presented) The array of claim 27, wherein the metal ions comprise silver ions.

50. (Previously presented) The array of claim 27, wherein at least one of the first and second electrodes is tungsten.

51. (Previously presented) The array of claim 27, wherein the metal layer comprises silver.

52. (Previously presented) The array of claim 27, wherein the chalcogenide glass layer comprises silver germanium sulfide.

53. (Currently amended) A memory array comprising:

at least one pair of memory cells, ~~the cells~~ each cell comprising ~~pillars~~ a pillar of stacked material layers [[on]] in contact with a shared conducting region of a semiconductor substrate, the stacked layers comprising a ~~shared~~ first electrode, ~~separate~~ a chalcogenide glass ~~layers~~ layer having metal ions diffused therein in contact with the ~~shared~~ first electrode and being capable of changing resistance under the influence of an applied voltage, ~~separate metal layers~~ a metal layer in contact

with ~~each of~~ the chalcogenide glass ~~layers~~ layer, and ~~separate~~ a second ~~electrodes~~ electrode in contact with ~~each of~~ the metal ~~layers~~ layer~~, the pillars not being located within vias~~.

54. (Previously presented) The array of claim 53, wherein the metal ions comprise silver ions.

55. (Currently amended) The array of claim 53, wherein at least one of the ~~shared~~ first ~~electrode~~ electrodes is tungsten.

56. (Previously presented) The array of claim 53, wherein at least one of the second electrodes is tungsten.

57. (Previously presented) The array of claim 53, wherein at least one of the metal layers comprise silver.

58. (Previously presented) The array of claim 53, wherein the chalcogenide glass layer having metal ions diffused therein comprises silver germanium sulfide.

59. (Currently amended) A processor system, comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising a memory array, the memory array comprising:

a plurality of memory units comprising stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode, a chalcogenide glass layer having metal ions diffused therein in contact with the first electrode and being capable of changing resistance under the influence of an applied voltage, a metal layer in contact with the chalcogenide glass layer, and a second electrode in contact with the metal layer, wherein the second electrode and metal layer comprise different materials~~, the at least one pillar not located within a via~~.

60. (Previously presented) The processor system of claim 58, wherein the metal ions comprise silver ions.

61. (Previously presented) The processor system of claim 58, wherein at least one of the first and second electrodes is tungsten.

62. (Previously presented) The processor system of claim 58, wherein at least one of the metal layers comprise silver.

63. (Previously presented) The processor system of claim 58, wherein the chalcogenide glass layer having metal ions diffused therein comprises silver germanium sulfide.